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MULTIBIT MEMORY CELL DESIGN USING MULTIPLE VALUED LOGIC

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Abstract: **The semiconductor market has been growing gradually over the long term, despite periodic troughs and peaks, and it is projected that this trend will continue in the years to come. The NAND Flash, which is designed for the data storage market, and the NOR Flash, which is addressing both the code and data storage segments due to its versatility, are the only types of Flash cells and architectures that can currently be considered industry standards. In this paper, a novel multibit flash memory cell is proposed. Multi valued logic allows for the storage of many bits in a single cell. The multilevel approach, where two bits are stored at the same level, should also be understood. The Multiple-Valued Logic system is one of the most promising approaches for achieving future beyond-binary electronics and systems. Multiple-valued logic can improve circuit connectivity, reduce chip space, and improve bus efficiency because more logic levels are used per line than in conventional binary logic. Mentor graphics software is used to assess the performance measures.**

Key Words: **Multi valued logic, Multibit Flash Memory**.

I. INTRODUCTION

Flash memory is frequently utilized in embedded systems to store data and programmed code. Since it is a non-volatile storage medium, data can be stored there without a power source. Flash memory can be electrically erasing and at the same time reprogramming the data. It rewrites data at the byte level and erases data in units known as blocks. Systems that constantly update data, like USB flash drives or SD cards, commonly use flash memory. A form of EEPROM, or electrically erasable programmable read-only memory, is flash memory. One of the numerous differences between EEPROM and Flash memory is how data is read, written, and erased. For instance, Flash memory and EEPROM having the capability to retrieve multi bit data at lower level and higher-level abstraction. The Flash memory cells are divided based on the kind of access—parallel or serial—and the programming and erasing mechanisms—Fowler-Nordheim tunnelling (FN), channel hot electron (CHE), hot-holes (HH), and source-side hot electron (SSHE)—as well as the access type.

Cells are the units of storage used by solid state memory systems to hold data. In accordance with conventional designs, each cell can only hold one bit of data at a time. An access transistor and a storage component, like a capacitor or floating gate, that stores data based on the electric charge on the storage component, are typically included in a cell. normal designs need for a single transistor for every bit of data since the electric charge in normal applications represents either a binary "1" or "0". Solid state memory storage density is determined by how tightly designers can arrange transistors on a semiconductor substrate. Although each new generation of transistors can be crammed closer together on a semiconductor substrate with each new generation of design technology, transistors can be crammed closer together, yet this density still falls short of a magnetic medium's storage density.

The first and second transistors are present in the flash memory cell. The first transistor has a floating gate, a drain connected to a data line, and a control gate connected to a word line. Similar to the first transistor, the second transistor has a second floating gate, a drain connected to a second data line, and a control gate connected to the word line. Prior to programming the flash memory cell, the second transistor's state is stored in the first floating gate. Additionally, the second floating gate stores the second transistor's preset state. an alteration in the states of the first

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and second transistors represents the value of the data stored in the flash memory cell.

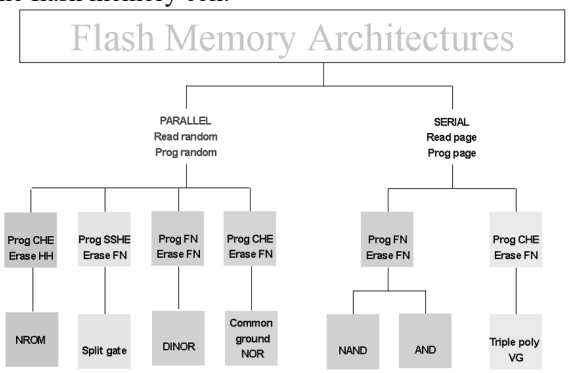

Fig:1 Flash memory tree representation

Based on the Parallel and Serial mode of operation used to Read the data and program the data from address lines as well as from pages the flash memories are considered as different types as shown in the figure 2.

II. BASIC IMPLEMENTATION METHODOLOGY

In floating gate memory, the state of the cell and the threshold voltage are changed by trapping or removing electrons from a floating polysilicon piece. When a read voltage is applied to the control gate, which is coupled to the word line, it senses the drain current of the MOSFET to determine the state of the cell. a single floating gate MOSFET makes up a binary flash memory cell. The cell's threshold voltage determines whether an action may be carried out, such as changing the cell's state or writing to its memory[1]. The two typical methods for modifying the cell's threshold voltage Channel Fowler-Nordheim Tunnelling for Programming, Hot Electron Injection for Programming, and Fowler-Nordheim Tunneling for Programming and for erasing.

As seen in Fig. 2, which depicts a transistor with a gate fully covered by dielectrics, the floating gate (FG), and electrically controlled by a capacitive coupled control gate (CG), a flash cell is essentially a floating-gate MOS transistor. The FG functions as the storing electrode for the cell device based on its internal structure. Charge injected into the FG is maintained, allowing for the adjustment of the "apparent" threshold voltage of the cell transistor. It goes without saying that the dielectrics' quality ensures non-volatility, while the thickness permits programming can use electrical pulses to destroy the cell [2]. Usually, the gate dielectric refers to the one between the transistor channel and the FG, which is an oxide in the 9–10 nm range and is known as "tunnel oxide" since it is between the transistor channel and the FG.

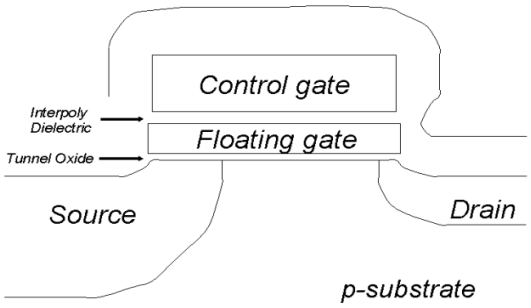

Figure2: Cross Sectional view of Flash Memory cell

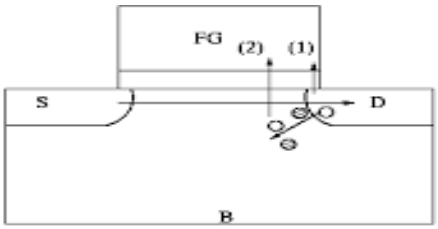

Figure3:Channel

Flash Memory cells can be programmed by hot electron injection. Channel When the source of a floating gate MOSFET is grounded and a high voltage is given to both the drain and the control gate, hot electron injection is used to programme the device. The hot electrons then flow beneath the floating gate. The increase in the device's threshold voltage is caused by the negative charge on the floating gate, which necessitates a greater potential difference for a channel to form between the source and drain. The device operates in this mode when it is being programmed.

The graphic depicts the process of erasing using FNT, which is carried out by pumping voltage to drive the wells. As a result of the high potential on the well contacts, electrons are attracted away from the floating gate and tunnel through the oxide in the direction of the well connections [3]. The device's threshold voltage decreases as a result of the elimination of charges from the floating gate, which triggers erase operation.

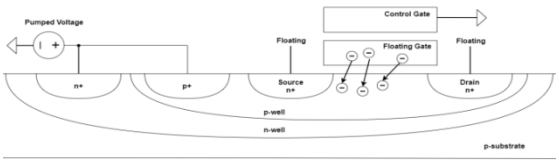

Figure 4: Fowler Nordheim Tunneling

The typical method for injecting FGs for analogue applications is to boost the source and gate voltage up much above Vdd in a way that makes it possible to know the channel current, as opposed to utilizing negative voltages

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for injection. If the drain is at a positive voltage, it will still provide a large enough Vsd to trigger injection. Significant infrastructure is needed for this process of "ramping up" all voltages related to floating gate transistors before lowering the drain to begin injection. It is important to design the infrastructure to be small, low-power, and simple to use, especially if all of the programming infrastructures are going to be integrated on the same chip.

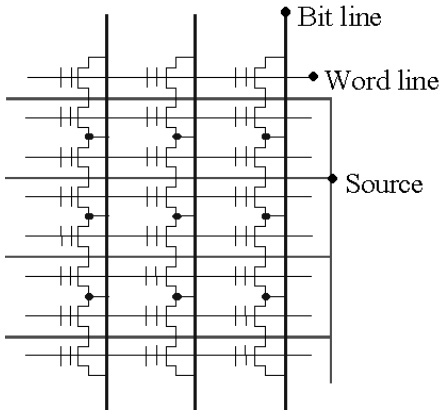

Figure5: NOR Flash array Structure

The ability to retrieve data in any order and without having to go through a set order of storage locations is what makes NOR Flash so well-suited for random access applications. Each memory cell in NOR Flash is connected in parallel, with one end to the source line and the other to the bit line, according to the design of the device. The system can now reach specific memory cells thanks to this Erasing the Flash data is equivalent to writing data "1" since injecting charge into the floating gate causes data "0" to be written and omitting charge causes data "1" to be written. A positively charged space charge region[4] will arise between the floating-gated cell's charge and the between the source and drain due to the induction of the floating gate, and the transistor will be on regardless of whether a bias voltage is applied to the control pole. When a proper bias voltage is applied to the control electrode to induce a charge on the silicon base, the source and drain of a transistor without charge in the floating gate can only conduct, meaning that the transistor is disabled when no bias voltage is applied to the control electrode.

III. MULTILEVEL CELL IMPLEMENTATION

When switching from traditional to ML Flash, the following three factors must be taken into consideration: In order to achieve narrow distributions, high programming accuracy is necessary. Reading operation also necessitates multiple comparisons—serial or parallel—with suitable references to ascertain the cell status, necessitating accurate and quick current sensing. Window and read voltage are also larger while read margins are smaller than in the single-bit case[9], which necessitates more reliable and/or error-correcting circuitry for all levels of allocation. The charge storage in multilevel cells changes depending on the threshold voltage value. The amount of charge that must be stored in the floating gate in order to place a memory cell's threshold voltage within any of a variety of voltage ranges that correspond to various logical levels. Bits can be stored in a cell that is operated at two separate levels; this is the case for the typical single-bit cell. Multilevel Cells are used in flash memory to hold more than two bits per cell.

A parallel sensing strategy can be employed to provide a quick reading operation in the NOR cell. Three currents produced by appropriate reference cells are simultaneously compared to the cell current obtained under reading conditions [9]. The binary code generated from the comparison results can contain the values 11, 01, 10, or 00 due to its multilayer nature.

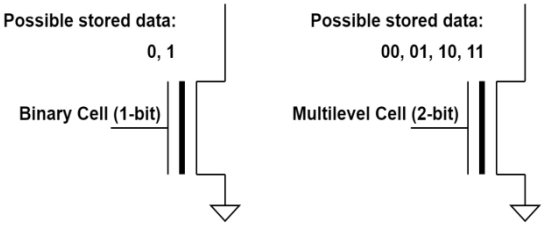

Figure6: Multibit Flash Memory cell

A flash memory cell can store n bits, but 2n-1 separate reference levels with precisely designed threshold voltages are needed for every n bits. As a result, there are 2n gaps between the reference threshold voltages. Low voltage values are now being taken into consideration in multi-bit memory cells as processes continue to get smaller. Accurate sensing is the secret to a flash memory that works [11].

One cause of mistake in Flash memory cells is an issue with data retention brought on by the device's threshold voltage changing due to the gradual leaking of charge off the floating gate. The retention age, which represents the length of time since the cell was last programmed, is used to characterize flash memory cells. At time t1, the cell's retention age was 1.The gadget is currently being used at the required voltage level, and the programme has just ended. The device threshold voltage has lowered from the final threshold voltage value from time t+ t1 to a new value that is lower than the final threshold voltage value.

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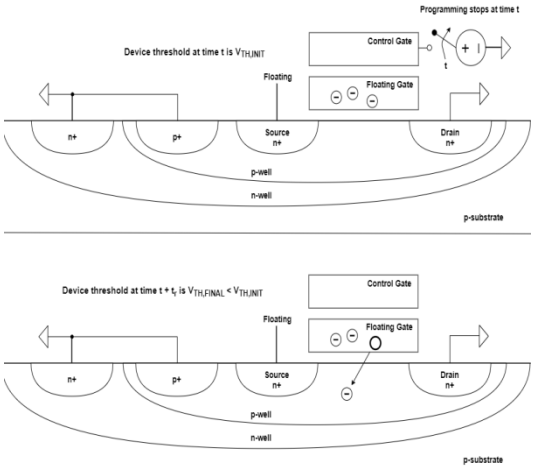


Figure 7: Charge leakage changes due to change in threshold voltage value

Flash memory reliability issues are referred to as read disturbances. The NAND flash design requires that every cell in a block that is not being read be read during read operations in order for the output signal to exit the block. Unwanted tunnelling is brought on by this voltage on the gate, which might alter the threshold and upset cells whose contents are not being read out. As the size of the transistors lowers, this effect gets stronger and stronger.

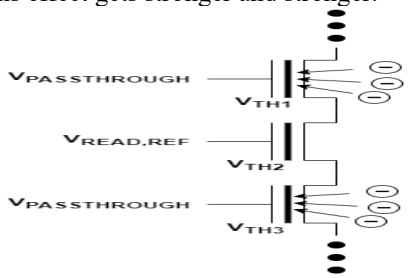


Figure 8:NAND Flash Read disturb

Sense amplifier plays a key role in reliable Flash memory-based circuits. Different types of sensing mechanisms like Serial, Parallel and Serial- parallel techniques are used to improve the accuracy of the Multibit Flash memory cell.

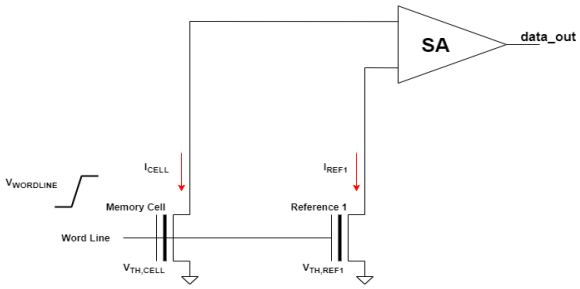


Figure9: Flash memory cell with sense amplifier

IV. IMPLEMENTATION OF MEMORY CELLS

The Multibit memory cell is constructed by instantiating the 1-bit memory cell. The data read and write operations are performed by using the write strobe signal. Based on the value of the write strobe signal it performs the hold operation or write operation. The performance metrics like delay, power dissipation and power delay product are verified.

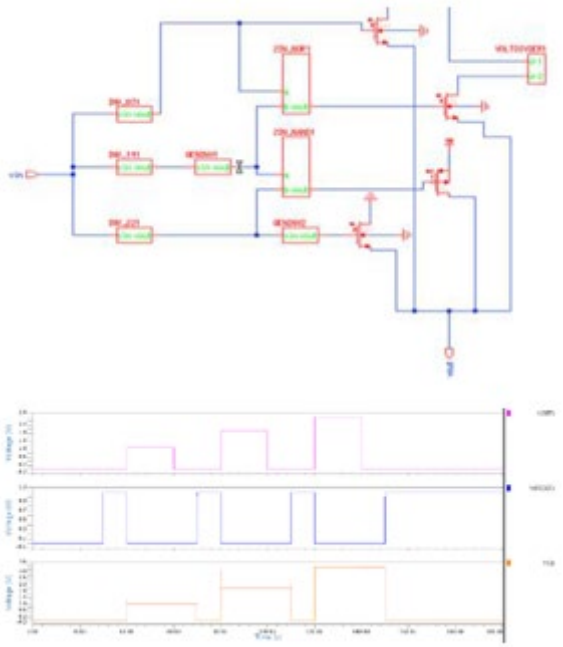
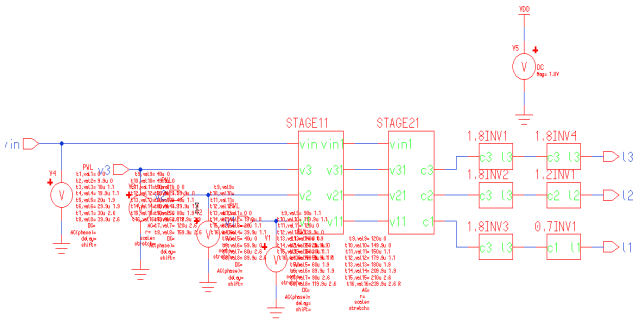


Figure10:Multibit Binary Memory cell and Output wave form

The Flash multibit flash memory memory cell is construced and verified the functional behaviour.The accuracy of the multibit cell is improved by compring it with single bit cell.The performance of the cell is improved by copmaring the prameters like power and delay [12].The physical design implementation of the Flash Memory cell is performed by Design Rule checking, Layout versus Schematic and GDSII implementation.



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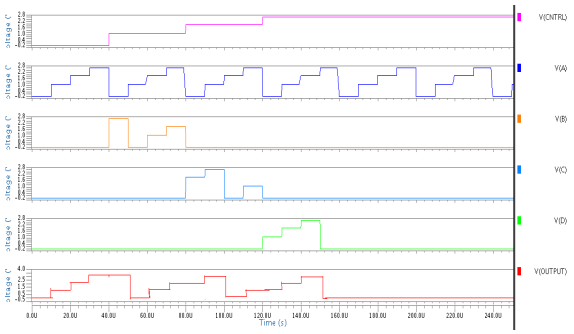

Figure11:Multibit Flash memory cell and output waveform

Comparison metrics:

Parameter	Binary SRAM cell[7]	Quaternary SRAM cell[7]	Flash Memory cell
Power	0.05427mW	0.47mW	0.52 mW
delay	98ns	56.6ns	38.4ns

V. CONCLUSION

The functional behaviour of the suggested Multibit Flash memory cell is confirmed. The installation of multi-bit cells employing quaternary logic to boost accuracy and reduce interconnects by resolving information in the fewest available bits was found to make flash memories faster than conventional memory. Quaternary memory modules' decreased propagation time suggests that they are more suited for high-speed applications. The MVL Logic-based circuits have fewer transistors, low power dissipation, and need less silicon area, making them better suited for implementing complex applications. Designs that were previously confined by the amount of functionality on a chip are now constrained by the amount of constrained power due to the technology's ongoing scalability. But this illustrates how quaternary-based memory are implemented.

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